Amendments to the Claims

Please amend the claims as follows:

1. (original) A method for routing a data frame through a fibre channel fabric, said fibre channel fabric comprising a switch having a plurality of ports, said ports are operative for transmitting and receiving said data frame, said method comprising:

receiving said data frame at a first port of said switch;

writing said data frame to a shared memory location, said shared memory location is coupled to at least two of said plurality of ports of said fibre channel switch;

identifying a second port of said switch, said second port operative for transmitting said data frame from said shared memory location;

transmitting a message from said first port to said second port indicating the position in said shared memory location of said data frame; and

at said second port, reading said data frame from said memory, wherein said switch has more than one rate for reading and writing data.

2. (original) The method of claim 1, wherein said shared memory location is implemented using a plurality of SRAM modules, one or more SRAM module for each of said plurality of fibre channel ports.

3. (original) The method of claim 2, wherein said plurality of fibre channel ports is an odd number of fibre channel ports.

4. (original) The method of claim 1, wherein said shared memory comprises a plurality of columns and wherein each of said plurality of fibre channel ports has access to one of said plurality of columns.

5. (original) The method of claim 4, wherein said access occurs during a clock cycle.

6. (original) The method of claim 4, wherein said access occurs during a 106.25 MHz clock cycle.

7. (original) The method of claim 4, wherein said plurality of columns comprises a plurality of SRAM modules.

8. (original) The method of claim 4, wherein said plurality of fibre channel ports have a read access during a first clock cycle and a write access during a second clock cycle, said second clock cycle immediately follows said first clock cycle.

9. (original) The method of claim 1, wherein said shared memory location supports both a 1 gigabit per second and a 2 gigabit per second read and write data rate.

10. (currently amended) A method for providing a shared memory location in a fibre channel fabric, said fibre channel fabric comprising a fibre channel switch having a plurality of fibre channel ports, said fibre channel ports are operative for transmitting and receiving [[said]] a data frame, said method comprising:

receiving said data frame at a first fibre channel port of said fibre channel switch;

writing said data frame in said shared memory location, said shared memory location coupled to each of said plurality of fibre channel ports; [[and]]

reading said data frame from said shared memory location into a second fibre channel port, wherein said fibre channel switch has more than one rate for reading and writing [[data.]] data; and

[[and]] transmitting said data frame to the second fibre channel port, wherein said writing and reading are performed in a manner that is dependent on the relative rates at which said frame is received and transmitted.

11. (currently amended) The method of claim 10, wherein said shared memory location is implemented using a plurality of SRAM modules, one or more SRAM ~~module~~ modules for each of said plurality of fibre channel ports.

12. (original) The method of claim 11, wherein said plurality of fibre channel ports comprises an odd number of fibre channel ports.

13. (original) The method of claim 10, wherein said shared memory location comprises a plurality of columns and wherein each of said plurality of fibre channel ports has access to one of said plurality of columns.

14. (original) The method of claim 13, wherein said access occurs during a clock cycle.

15. (original) The method of claim 13, wherein said access occurs during a 106.25 MHz clock cycle.

16. (original) The method of claim 13, wherein said plurality of columns comprises a plurality of SRAM modules.

17. (original) The method of claim 13, wherein said plurality of fibre channel ports have a read access during a first clock cycle and a write access during a second clock cycle, said second clock cycle immediately follows said first clock cycle.

18. (original) The method of claim 10, wherein said shared memory location supports both a 1 gigabit per second read and write data rate and a 2 gigabit per second read and write data rate.

Please cancel claims 19-42.

19-42. (cancelled)